CLAIMS:

1. A LC-Display with n gate drivers (GD) and a source drivers (SD) for driving a Display with dots arranged in x rows (Rx) and y columns (Cy), the gate driver (GDn) has several output stages (OUTx) for driving the gate lines (GLy) of the display, characterised in that, an additional voltage line (VLclean) is provided, which is coupled to the output stages (OUTx) of the gate driver (GDn).

2. Display as claimed in claim 1, whereas the output stage is provided with a PMOS and two NMOS transistors and the PMOS transistor (MP1) is arranged between the supply line VH and the output (OUTx) of the output stage and the first NMOS transistor MN1 is arranged between the supply line (VL) and the output (OUTx) of the output stage and the second NMOS transistor (MN2) is arranged between the supply line (Vlclean) and the output (OUTx) of the output stage.

3. Display as claimed in claim 1, whereas the additional supply line (VLclean) is routed over a separate track from VL-potential.

4. Display as claimed in claim 1, whereas the track of the supply line (VL) and the track of the supply line (VLclean) are coupled to the same supply level.

5. Display as claimed in claim 1, whereas the track of the supply line (VL) and the track of the supply line (VLclean) are connected together in a location where the track impedance to the supply circuit's output is low.

6. Method for driving a display with n gate drivers (GDn) and at least one source driver (SD), whereas dots are arranged in x rows (Rx) and y columns (Cy), the gate driver (GDn) has several output stages (OUTx) for driving gate lines (GLy) of the display and a capacitance (Cst) of the selected gate line (GLy) is connected to the

previous gate line (GLy-1) characterised in that, an additional supply line (Vlclean) of the output stage for row (GLy) is activated when the row (GLy+1) is activated.

7. Method for driving a display with n gate drivers (GD) and a source driver (SD), whereas dots are arranged in x rows (Rx) and y columns (Cy), the gate driver (GDn) has several output stages (OUTx) for driving the gate lines (GLy) of the display and a capacitance (Cst) of the selected gate line (GLy) is connected to the next gate line (GLy+1), characterised in that, an additional supply line (Vlclean) of the output stage for row (GLy) is activated when (GLy+1) is activated.